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(54) **Method for controlling the sheet resistance of thin film resistors**

(57) A method for controlling the sheet resistance of thin film resistors. The sheet resistance can be inexpensively controlled within a tight tolerance by determining a desired final value for the sheet resistance of thin film resistor material to be deposited on a substrate, depositing the resistor material on the substrate using a deposition process which is consistent enough to achieve a target sheet resistance within a first specified toler-

ance, the resistor material being deposited to achieve a target sheet resistance which is equal to the desired final value minus the first specified tolerance, and removing a small amount of material from the surface of the deposited thin film resistor material by etching or ion bombardment to raise the sheet resistance to the desired final value within a second specified tolerance characteristic of the removing process where the second specified tolerance is less than the first specified tolerance.

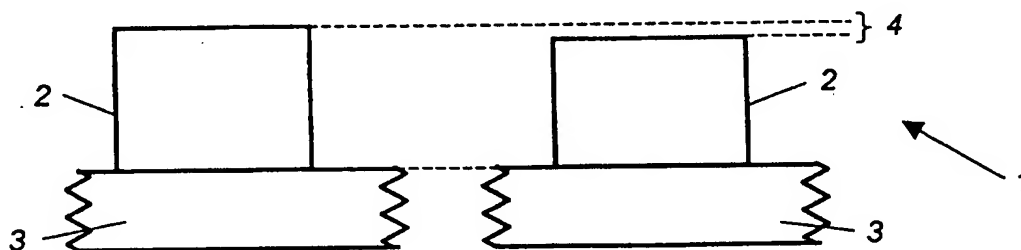


Figure 1A

Figure 1B

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Description

Technical Field

[0001] A method for producing thin film resistors to a tighter sheet resistance specification.

Background and Summary

[0002] Thin film resistors are used in most GaAs and InP devices and integrated circuit fabrication processes, in thin-film substrate manufacturing, and in some Si processes. The resistor sheet resistance typically has a specified tolerance of $\pm 15\%$, although with special care in fabricating the thin film resistors, the resistor sheet can be controlled to $\pm 10\%$. However, for many integrated circuit designs it would be of a great advantage to be able to control the sheet resistance to a much tighter tolerance. This is especially true in very high speed integrated circuits where resistor values need to be controlled well in impedance matching circuitry.

[0003] One method of achieving tight control of the resistor sheet resistance is to re-process any thin film that does not have the desired sheet resistance by stripping the thin film and re-depositing it. However, such a procedure essentially doubles the cost of processing the thin film resistor. Therefore, a need exists for inexpensively controlling the sheet resistance of thin film resistors to within a tight tolerance of their targeted value.

[0004] The present invention addresses this need. More particularly, a disclosed method of the invention improves the tolerance of thin film resistors to within $\pm 3\%$ or better with minimum additional processing expense. To this end, the disclosed method for controlling the sheet resistance of thin film resistors comprises determining a desired final value for the sheet resistance of thin film resistor material to be deposited on a substrate. The thin film resistor material is deposited on the substrate using a deposition process which is consistent enough to achieve a target sheet resistance for the deposited thin film resistor material within a first specified tolerance. The thin film resistor material is deposited by the deposition process to achieve a target sheet resistance which is equal to the desired final value minus the first specified tolerance. A small amount of material is then removed from the surface of the deposited thin film resistor material by an etching or ion bombardment process to raise the sheet resistance to the desired final value within a second specified tolerance characteristic of the etching or ion bombardment process, where the second specified tolerance is less than the first specified tolerance. The etching process employed in a preferred embodiment uniformly removes material from the surface of the deposited thin film resistor by argon sputter etching.

[0005] According to the disclosed, preferred embodiment, the method further comprises, after the thin film resistor deposition, measuring the sheet resistance of

the deposited thin film resistor material by measurement or calculation, determining the thickness of the deposited thin film resistor material, calculating the thickness of the deposited thin film resistor material needed to be removed to raise the sheet resistance to the desired final value, and calculating the time for performing the removing process to remove the calculated thickness needed to be removed based on a measured removal rate for the removing process. Further, the method includes patterning a thin film resistor from the thin film resistor material on the substrate. The patterning can be performed before or after the sheet resistance is raised to the desired final value. The invention advantageously permits the thin film resistor sheet resistance on critical integrated circuit designs to be controlled to better than $\pm 3\%$ with minimum additional processing expense.

[0006] These and other objects, features and advantages of the present invention will become more apparent from the following description of a preferred embodiment of the invention.

Brief Description of the Drawings

[0007] Fig. 1A is an enlarged side view of a substrate with a thin film resistor material deposited thereon according to the invention to achieve a target sheet resistance R_s which is equal to a desired final value for the sheet resistance minus a specified tolerance of the deposition process.

[0008] Fig. 1B is an enlarged side view of the substrate with thin film resistor material of Fig. 1A after removal of a small amount of material uniformly from the surface of the thin film resistor material by argon sputter etching the material to raise the sheet resistance thereof to the desired final value within a specified tolerance of the etching process.

[0009] Fig. 2 is a flow chart of steps in a method of the invention, Process 1 on the left side being for the case where the resistor material is patterned before the sheet resistance is adjusted to within $\pm 3\%$ or better and Process 2, on the right side of the flow chart, being for the case where the resistor material is patterned after the sheet resistance is adjusted.

Detailed Description

[0010] Referring now to the drawings, a thin film resistor 1 made according to the method of the invention is depicted in Figure 1B. The resistor 1 comprises a thin film resistor material 2 supported on a substrate/wafer 3. The thin film resistor can form part of a very high speed integrated circuit such as a GaAs or InP integrated circuit device. The method of the invention for forming the thin film resistor 1 includes first depositing the thin film resistor material 2 on the substrate 3 at a sheet resistance that is less than the desired final value. See Fig. 1A. The resistor material is deposited by evaporation or sputter deposition. For example, if the deposition

process is consistent enough to achieve the target sheet resistance within $\pm 10\%$, the thin film resistor material 2 is deposited at a sheet resistance equal to 90% of the desired final value. This results in all initial thin film sheet resistances being in a range of 80% to 100% of the desired final sheet resistance.

[0011] The sheet resistance is raised to its final value by etching, preferably using an Ar sputter etch or an ion bombardment to remove a small amount of material, the thickness of which is denoted at 4 in Figure 1B, from the surface of the thin film resistor. This is accomplished by first measuring the thin film resistor sheet resistance, then etching the thin film resistor in the argon sputter etch for a time that has previously been calibrated. Since it is possible to controllably remove material in the argon sputter etch to within a few angstroms, the thin film resistor sheet resistance can be controlled routinely to within $\pm 3\%$ of its target value.

[0012] The resistor material 2 in the disclosed embodiment is NiCr, but the process is applicable to all types of thin film resistor material, such as other high resistivity materials including TaN, CrSi and CrSiO, as well as lower resistivity materials including Ti, TiSi₂, W, Mo, Au, Ag and various metals. The thickness of the thin film resistor material 2 can range from less than 50 Å to in excess of 50,000 Å. The initial sheet resistance of the deposited material 2 on the substrate in Figure 1A can be greater than 10⁶ ohms/square to less than 0.1 ohm/square, depending upon the design criteria. The desired final value for the sheet resistance is whatever has been specified as the target value and as noted above has a typical specified tolerance of about $\pm 15\%$, with an actual range of more like $\pm 10\%$.

[0013] Argon is the preferred sputter etch gas, but the process of the invention is amenable to the use of any other gas which can remove the resistor material by etching or by ion bombardment. The argon sputter etch conditions are adjusted for the sputter etch system to provide a uniform etch at an etch rate that will take off the required amount of material in a reasonable time, e. g., within a range of about 10 seconds to several minutes. Conditions of the sputter etch vary considerably depending on whether the etch system is a single wafer machine or a batch machine. An example of ranges for typical process parameters are: power, tens of watts to greater than 1,000 watts; voltage, tens of volts to 100s of volts; pressure, tens of μ Torr to several Torr; and gas flow, less than 10 cc/min to greater than 100 cc/min.

[0014] The parameters are preferably adjusted to remove less than .1 % to greater than 3% of the total resistor material in about 10 seconds. Similar etch rates would be desirable for any other material used to ion bombard or chemically etch the thin film resistor material.

[0015] To establish a calibrated etch time to achieve a desired final thin film sheet resistance for the resistor 1 in Figure 1B after deposition, the sheet resistance of the thin film resistor material 2 in Figure 1A is measured.

The thickness of the thin film resistance material in Figure 1A is then determined, either by measurement or calculation based upon its thickness assuming a fixed resistivity. The thickness 4 of the resistance material that must be removed to achieve the final target sheet resistance value is then calculated. The time that the thin film resistor material 2 must be etched to remove the thickness 4 is then calculated based on the previously measured etch rate of the sputter etch (or chemical etch) employed for removing the resistor material. These steps are shown in the flow chart of Figure 2. Process 1, depicted by thin film resistor cross sections in Figures 1A and 1B, therein indicates that the resistor can be patterned on the substrate before the sheet resistance is adjusted to within $\pm 3\%$ or better. Process 2 patterns the resistor after the sheet resistance is adjusted.

[0016] The method of the invention enables the integrated circuit manufacturer to control thin film resistor sheet resistance to within a tight tolerance of the target value with minimum additional processing expense. The invention can be used to control the sheet resistance of thin film resistors on any type of integrated circuit or substrate that uses thin film resistors in its circuitry.

[0017] While I have shown and described only one embodiment of the present invention herein, it will be readily understood by the skilled artisan that variations of the method for controlling the sheet resistance of thin film resistors are possible without departing from the scope of my invention. Therefore, I do not wish to be limited to the details shown and described herein but intend to cover all such chances and modifications as are encompassed by the scope of the appended claims.

Claims

1. A method for controlling the sheet resistance of thin film resistors, comprising:

determining a desired final value for the sheet resistance of thin film resistor material to be deposited on a substrate,
deposited said thin film resistor material on said substrate using a deposition process which is consistent enough to achieve a target sheet resistance for the deposited thin film resistor material within a first specified tolerance, said thin film resistor material being deposited by said deposition process to achieve a target sheet resistance which is equal to said desired final value minus said first specified tolerance, and
removing a small amount of material from the surface of the deposited thin film resistor material by one of an etching and ion bombardment removing process to raise the sheet resistance to said desired final value within a second specified tolerance characteristic of said removing

process, said second specified tolerance being less than said first specified tolerance.

2. The method according to claim 1, further comprising, after said depositing, measuring the sheet resistance of said deposited thin film resistor material, determining the thickness of said deposited thin film resistor material, calculating the thickness of said deposited thin film resistor material needed to be removed to raise the sheet resistance thereof to said desired final value, and calculating the time for performing said removing process to remove said calculated thickness based on a measured removal rate for said removing process. 5
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3. The method according to claim 2, wherein said determining the thickness of said deposited thin film resistor material is accomplished by measuring the deposited thin film resistor material. 20
4. The method according to claim 2, wherein said determining the thickness of said deposited thin film resistor material is accomplished by calculation using said measured sheet resistance and a reference characteristic for said material relating thickness and sheet resistance. 25
5. The method according to claim 1, and further comprising 30

patterning a thin film resistor from said thin film resistor material on said substrate.
6. The method according to claim 5, wherein said patterning is done before the sheet resistance is raised to said desired final value. 35
7. The method according to claim 5, wherein said patterning is done after the sheet resistance is raised to said desired final value. 40
8. The method according to claim 1, wherein: 45

the deposition process is selected from the group consisting of evaporation and sputter deposition.
9. The method according to claim 1, wherein said small amount of material is removed uniformly from said surface of the deposited thin film resistor material in a time within the range of from about 10 seconds to several minutes. 50
10. The method according to claim 1, wherein: 55

the substrate is a GaAs or InP integrated circuit substrate.

11. The method according to claim 1, wherein:

the removing step includes an Argon sputter etching.

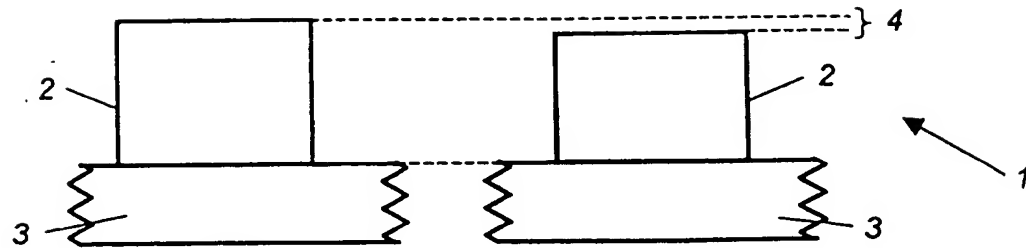
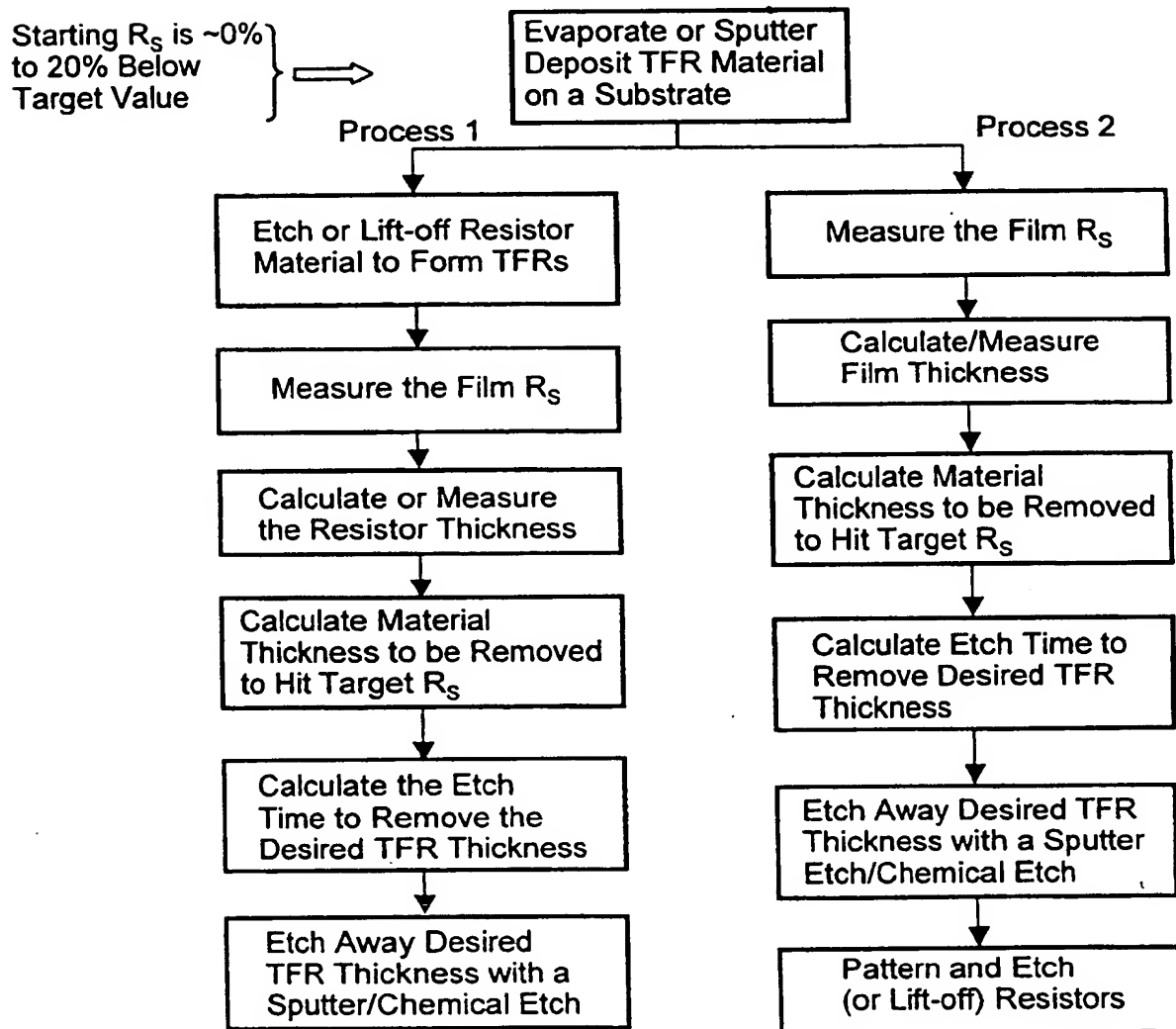


Figure 1A

Figure 1B





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 02 00 4247

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	"IN SITU-TRIMMED FINE-GRAINED POLYSILICON RESISTORS" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 33, no. 5, 1 October 1990 (1990-10-01), pages 280-281, XP000107465 ISSN: 0018-8689	1,9	H01C17/24 H01L21/02
Y	* page 280, line 18 - page 281, line 17 *	2-4	
A	---	5-7,10, 11	
Y	EP 0 070 809 A (SELENIA IND ELETTRONICHE) 26 January 1983 (1983-01-26) * page 2, line 17 - line 25; claim 1 *	2-4	
A	---	5-7	
A	GB 2 207 546 A (BRITISH TELECOMM) 1 February 1989 (1989-02-01) * page 4, line 1 - line 5 *	8,10	
A	---	11	
A	US 6 191 026 B1 (RANA VIRENDRA V S ET AL) 20 February 2001 (2001-02-20) * column 2, line 37 - line 38 * * column 4, line 42 - line 67 *		TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01C H01L
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 7 June 2002	Examiner Frias Rebelo, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 02 00 4247

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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07-06-2002

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 0070809	A	26-01-1983	IT EP	1171401 B 0070809 A2	10-06-1987 26-01-1983
<hr/>					
GB 2207546	A	01-02-1989	NONE		
<hr/>					
US 6191026	B1	20-02-2001	JP	9219401 A	19-08-1997
<hr/>					

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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